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CLEAN VERSION PENDING CLAIMS

SEMICONDUCTOR MEMORY WITH WORDLINE TIMING
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Claims 43-67 and 70-88, as of November 14, 2002 (Date of Response to First Office Action).

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43. (Amended) A timing circuit, comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal; and

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal.

44. The timing circuit according to claim 43, wherein the at least one input signal includes a RAS* signal.

45. The timing circuit according to claim 44, wherein the output activates the address decoder based on a low RAS* signal and a low isolation signal.

46. The timing circuit according to claim 45, wherein the isolation signal is associated to a first memory array separate from a second memory array connected to the address decoder.

47. The timing circuit according to claim 43, wherein the input is connected to a NOR gate.

48. The timing circuit according to claim 43, wherein the input is connected to an AND gate.

49. (Amended) A timing circuit connected to a wordline decoder of a first memory array, the timing circuit comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal connected to a sense amplifier for a second memory array; and

an output connected to the wordline decoder, wherein the timing circuit activates the wordline decoder based on the at least one input signal.

50. The timing circuit according to claim 49, wherein the at least one input signal includes a RAS* signal.

51. The timing circuit according to claim 50, wherein the output activates the wordline decoder based on a low RAS* signal and a low isolation signal.

52. The timing circuit according to claim 49, wherein the input is connected to a NOR gate.

53. The timing circuit according to claim 49, wherein the input is connected to an AND gate.

54. The timing circuit according to claim 49, wherein the first memory and the second memory array are connected to one sense amplifier.

55. A memory device comprising:

a plurality of memory cells coupled to digit lines;

a sense amplifier;

a plurality of isolation gates coupled between the sense amplifier and the digit lines, the isolation gates being controlled by isolation signals;

a timing circuit connected to one of the plurality of isolation gates; and

a wordline decoder connected to the timing circuit and at least one of the memory cells, wherein the timing circuit triggers the wordline decoder upon a state change in isolation signal at the one isolation gate.

56. The memory device according to claim 55, wherein the timing circuit is connected to a RAS* signal and activates the wordline decoder based on both the isolation signal and the RAS* signal shifting low.

57. The memory according to claim 56, wherein the isolation signal experiences a delay from its source to the isolation gate relative to the RAS* signal.

58. A memory device comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

59. The memory device according to claim 58, wherein the first timing circuit receives a RAS* signal, and based on the RAS* signal and the state of the first isolation signal selectively activates the second wordline decoder.

60. The memory device according to claim 58, wherein the second isolation line transmits a second isolation signal to the second isolation gate, and a second timing circuit is connected to

the second isolation line and the first wordline decoder and activates the first wordline decoder based on a change of state of the second isolation signal.

61. The memory device according to claim 60, wherein the second timing circuit receives a RAS* signal and based on the RAS* signal and the state of the second isolation signal selectively activates the first wordline decoder.

62. The memory device according to claim 60, wherein the plurality of sense amplifier banks includes N sense amplifier banks and N first isolation gates, plurality of memory arrays includes N * 2 memory arrays, and a number of first timing circuits equals N, and the number of second timing circuits is N.

63. The memory device according to claim 58, wherein the memory device is one of a DRAM, SRAM, Flash memory, SGRAM, SDRAM, SDRAM II, DDR SDRAM, Synchlink DRAM, and Rambus DRAM.

64. A computer, comprising:

a processor;

a plurality of memory arrays coupled to the processor, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory

arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

65. An integrated circuit, comprising:

a semiconductor wafer having first and second surfaces; and

a functional circuit formed on the first surface of the semiconductor wafer, the functional circuit including:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

66. An electronic system, comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of memory arrays, each memory array including a plurality of

memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

67. The electronic system according to claim 66, wherein the processor includes a user interface device.

70. (New) An integrated circuit, comprising:

a memory array,

a plurality of sense amplifiers operably connected to the memory array,

an isolation gate operably connected between the memory array and the sense amplifiers, and

a timing circuits operable connected to the isolation gate, comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal; and

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal.

71. (New) A timing, integrated circuit, comprising:

an input adapted to receive a row access signal and a sense amplifier isolation signal; and

an output adapted to connect an address decoder, wherein the timing circuit activates the address decoder based on a state of the row access signal and the sense amplifier isolation signal.

72. (New) The timing, integrated circuit according to claim 71, wherein the output presents an activation signal to the address decoder based on the row access signal being low and the sense amplifier isolation signal being low.

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73. (New) The timing, integrated circuit according to claim 72, wherein the input includes a NOR gate.

74. (New) The timing, integrated circuit according to claim 72, wherein the input includes an AND gate.

75. (New) An integrated circuit adapted to time activation of a wordline decoder to a sense amplifier isolation signal, comprising:

a first input connected to a sense amplifier isolation signal line;

a second input adapted to receive a memory access control signal;

an output adapted to activate/deactivate a wordline decoder based on the first input and the second input.

76. (New) The integrated circuit of claim 75, wherein the second input receives a row access strobe signal.

77. (New) The integrated circuit of claim 75, wherein the second input receives a low, active signal.

78. (New) The integrated circuit of claim 75, further comprising a logic element that produces an output signal on the output based on the first input and the second input.

79. (New) A timing circuit, comprising:

a delay circuit connected to a sense amplifier isolation signal line;

a first input connected to the delay circuit;

a second input adapted to receive at least one input signal; and

an output based on the first input and the second input and connected to an address decoder, wherein the timing circuit activates the address decoder based on the first input signal and the second input signal.

80. (New) The timing circuit of claim 79, wherein the delay circuit includes a programmable delay.

81. (New) The timing circuit of claim 80, wherein the programmable delay is within a range of programmable delay times.

82. (New) The timing circuit of claim 81, wherein the range of programmable delay times represents the propagation time of a sense amplifier isolation signal on the sense amplifier signal line.

83. (New) The timing circuit of claim 79, wherein the delay circuit is adapted to produce a delay based on a propagation time of an isolation signal.

84. (New) The timing circuit of claim 79, wherein the delay circuit is adapted to produce a delay based on a signal required for accessing a wordline, column or memory location in a memory device.

85. (New) An integrated circuit adapted to time activation of a wordline decoder to a sense amplifier isolation signal, comprising:

a first input adapted to receive a sense amplifier isolation signal;

a second input adapted to receive a memory access control signal;

a timing output adapted to activate/deactivate a wordline decoder based on the first input and the second input.

86. (New) The integrated circuit of claim 85, wherein the first input is active, the second input is inactive and the timing output is inactive.

87. (New) The integrated circuit of claim 86, wherein the first input is active at a high state and the second input is active at a low state.

88. (New) The integrated circuit of claim 85, wherein the timing output produces an active signal with the first input being low and the second input being low.